FP 15.4: A 450MHz IA32 P6 Family Microprocessor

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A 1.4V to 2.2V 450MHz CMOS 7.5M transistor microprocessor in 131mm^2 makes use of a five-layer-metal 0.25µm process technology. This is the third generation implementation of this microprocessor. This microprocessor implements the full Intel instruction set, including MMX(TM) Technology instruction set extensions [1, 2]. This implementation adds new support for back side bus caches that transfer data at the core clock rate in 1MB and 2MB implementations to support 4-way servers [3].

Table 1 compares the process features and silicon results of this microprocessor on 0.25µm process technology, with the previous implementation on 0.35µm process technology [4]. The 0.25µm process technology has a fifth layer of metal to enable RC delay and area reductions. This fifth layer of metal permits reduction of channel area between blocks by over 50%. The remaining space in between blocks is used to add bypass capacitors. Bypass capacitors are also added inside of circuit blocks where possible. Additional bypass capacitors are added under the wire bonding pads to provide bypassing for the output drivers. The total on-die bypass capacitance is approximately 117nF.

The fifth layer of metal also supports C4 bumps. This die supports both wire bonding and C4 packages. The C4 package is a 31mm square using organic land grid array technology. The wire bond package is a plastic land grid array 42.5mm square. Neither package requires in-package bypass capacitance. Figure 1 is a section of the I/O ring that shows the wire bonding pads and the C4 bumps. The C4 bump pitch used is 272µm and the wire bond pad pitch is 68µm.

The benefit of C4 packaging combined with on die decoupling capacitance results in reduced power supply noise at the silicon level. Clock distribution delay is modulated by Vcc noise, which contributes jitter. The measured 90ps peak-to-peak long-term jitter of the I/O clock demonstrates the results. Figure 2 shows the I/O clock jitter relative to the external clock over a large number of cycles, while the part undergoes stop clock operation.

The combination of the addition of the fifth layer of metal and the larger aspect ratios of the metal lines results in good RC management. The line-to-line coupling however is increased dramatically and results in significant noise coupling and associated circuit risk. A methodology extracts line-to-line parasitics for all signal lines on the microprocessor. Coupling ratios are combined with timing information to determine which signals are at risk of noise induced speed degradation or functional failures. There is no indication of any line-to-line coupling-induced failures in silicon testing. The methodology for finding and fixing cross coupling violations will be described in detail, for both static and domino logic.

Scaling of the transistor channel length permits voltage operation from 1.4V to 2.2V. All circuitry is simulated for operation from 1.2V to 2.8V. The peak power is 18.9W at 450MHz at 2.0V running a worst case pattern. The power at 1.6V and 266MHz is 7.15W peak. Typical office application software power dissipation is not close to worst-case and is about 4W at 266MHz at 1.6V.

On-die clock skew is difficult to manage and reduces the maximum clock rate. This design distributes the clock with matched delay lines to the right and left side of the die. Local variations in Vcc and Leff result in increases to clock skew that can not be compensated for with layout. A tunable delay line circuit is added to the matched clock tuning paths, that detects the skew offset from the left and right side and compensates to reduce skew [5].

The on-die cache bit-line sensing differential voltage is reduced to 85mV. Programmable timing generators allow sensing margin adjustment. This feature permits ease in characterization. Variability in sense amp offset, bit-line signal development, and weak cells, can all be detected with this same mechanism in production testing with short test times. The feature is enabled through JTAG.

Two types of caches are supported on the back side bus. The first type supports the desktop and is comprised of PBSRAMs and a TAGRAM (Figure 3). 256kB and 512kB sizes are supported. The transfer rate to the microprocessor is ½ of the microprocessor clock rate. The second type of cache is optimized for servers and work stations, and is comprised of proprietary cache RAMs that permit cache sizes of 1MB and 2MB (Figure 4). These proprietary cache RAMs have duplicate on-board TAGRAMs. The data transfer rate is at the full microprocessor clock rate, which is 3.6GB/s at 450MHz. Both cache variants use standard component packages and are implemented on FR4 substrates.

Front side bus-to-core clock rate ratios are added to support the higher core clock rate and front side bus speeds faster than and including 66MHz. The new fractions are 2/9 and 1/5. GTL+ at 1.5V is supported. Legacy signals at 2.5V are also supported with on-chip capacitive dividers. This technique is also used on the clock input.

Figure 6 is a die micrograph with all metal layers.

References:

[1] Colwell, R., et al., "A 0.6mm BiCMOS Processor with Dynamic Execution," ISSCC Digest of Technical Papers, pp. 176-177, Feb., 1995.

[2] Choudhury, M. et. al., "A 300 MHz CMOS Microprocessor with Multi-Media Technology," ISSCC Digest of Technical Papers, pp. 170-171, Feb., 1997.

[3] Halbert, John, et. al., "A 450MHz 512kB Second Level Cache with a 3.6GB/s Data Bandwidth," ISSCC Digest of Technical Papers, Feb., 1998.

[4] Bohr, M., "A High Performance 0.25 micron Logic Technology Optimized for 1.8v Operation," IEDM Technical Digest, pp. 847-851, Dec., 1996.

[5] Geannopoulos, G., et. al., "An Adaptive Digital Deskewing Circuit for Clock Distribution Networks," ISSCC Digest of Technical Papers, Feb., 1998.

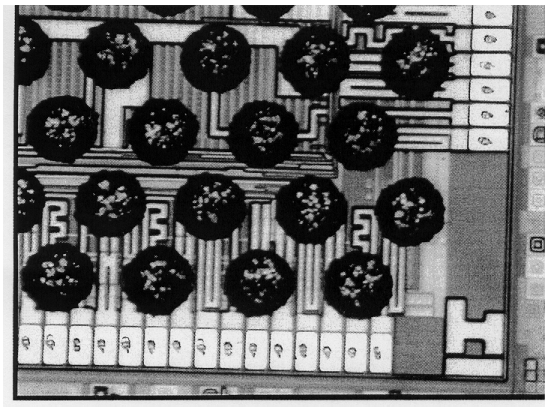


Figure 1: Section of I/O ring.

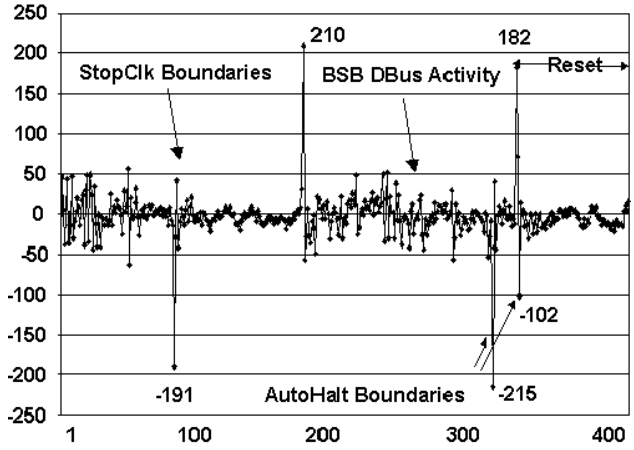


Figure 2: I/O clock jitter with stop clock

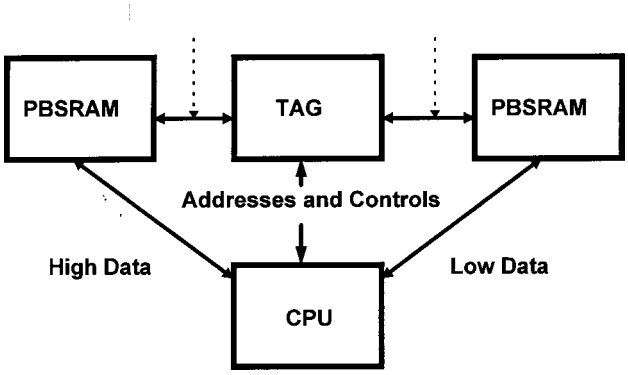


Figure 3: PBSRAM back side bus cache.

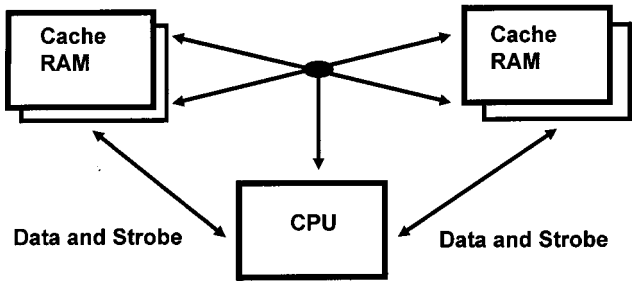


Figure 4: Cache RAM back side bus cache.

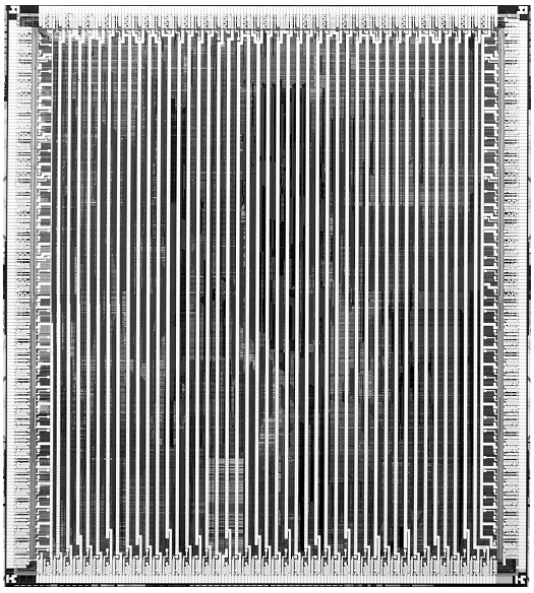
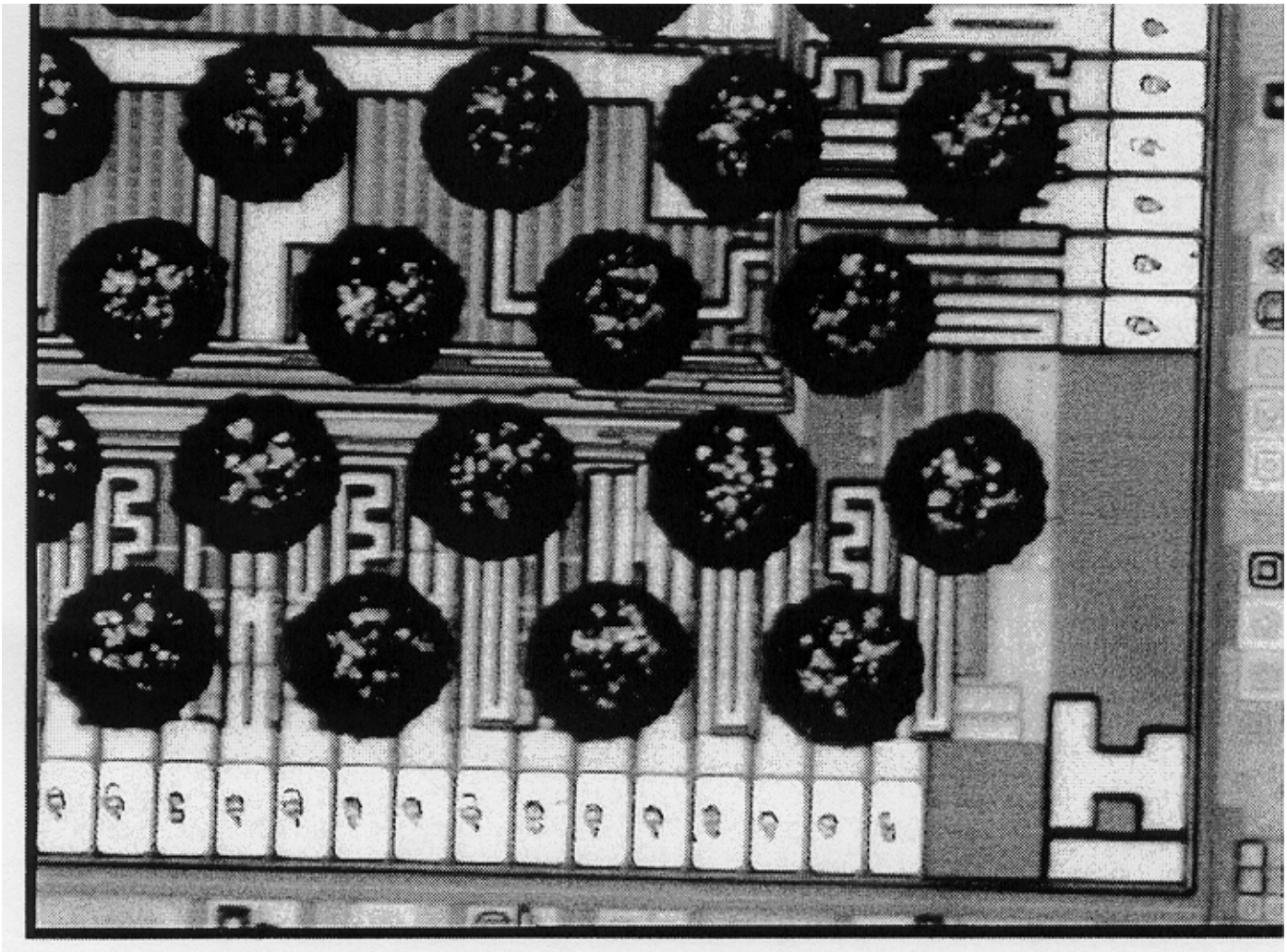


Figure 5: Die micrograph with all metal layers.

		0.35 μm	0.25 μm
Supply Voltage	(V)	2.8	2
Clock rate	(MHz)	300	450
Die Area	(mm2)	203	131
Metal 1 pitch	(μm)	0.88	0.64
Metal 2 pitch	(μm)	1.16	0.93
Metal 3 pitch	(μm)	1.16	0.93
Metal 4 pitch	(μm)	3.04	1.6
Metal 5 pitch	(μm)	n/a	2.56
Leff	(μm)	0.22	0.14
Tox	(nm)	6	4

Table 1: 0.25μm vs. 0.35μm processes.



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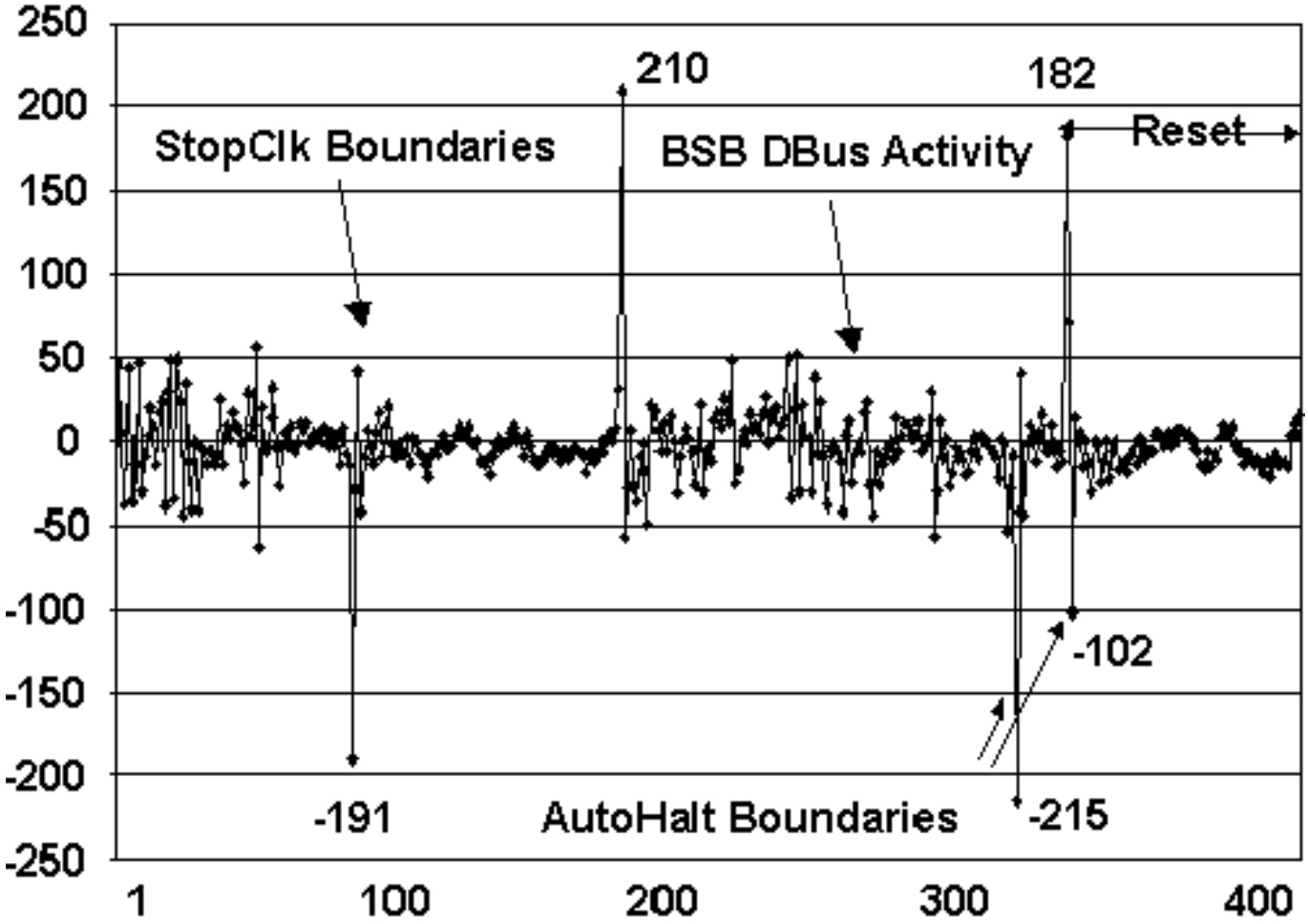

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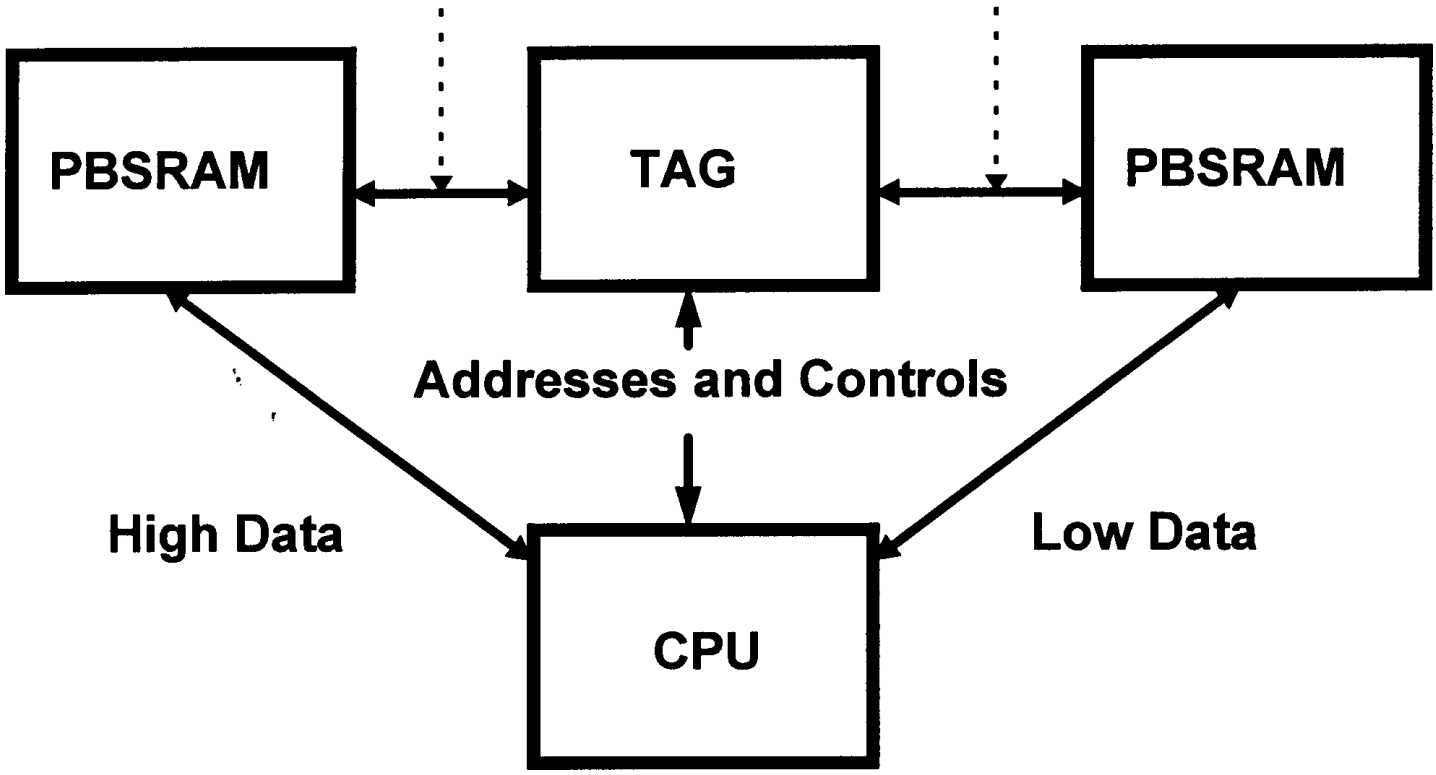


Figure 3: PBSRAM back side bus cache.

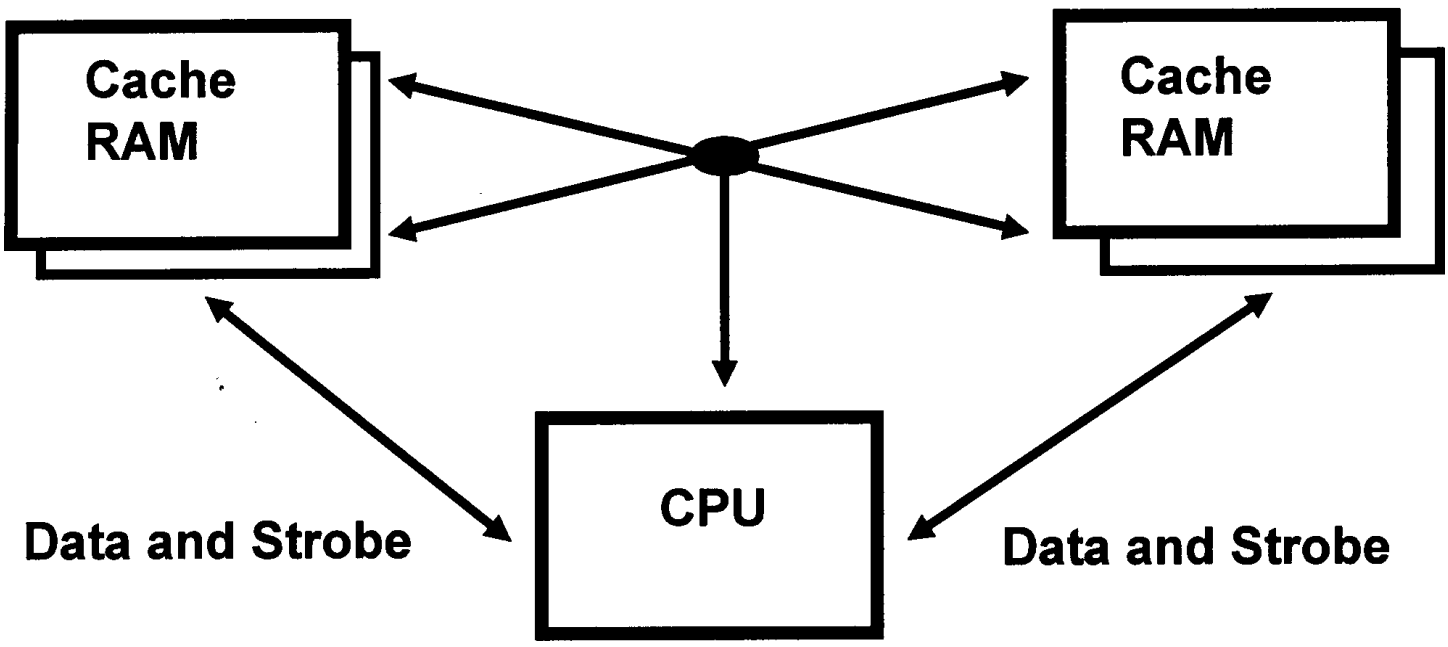
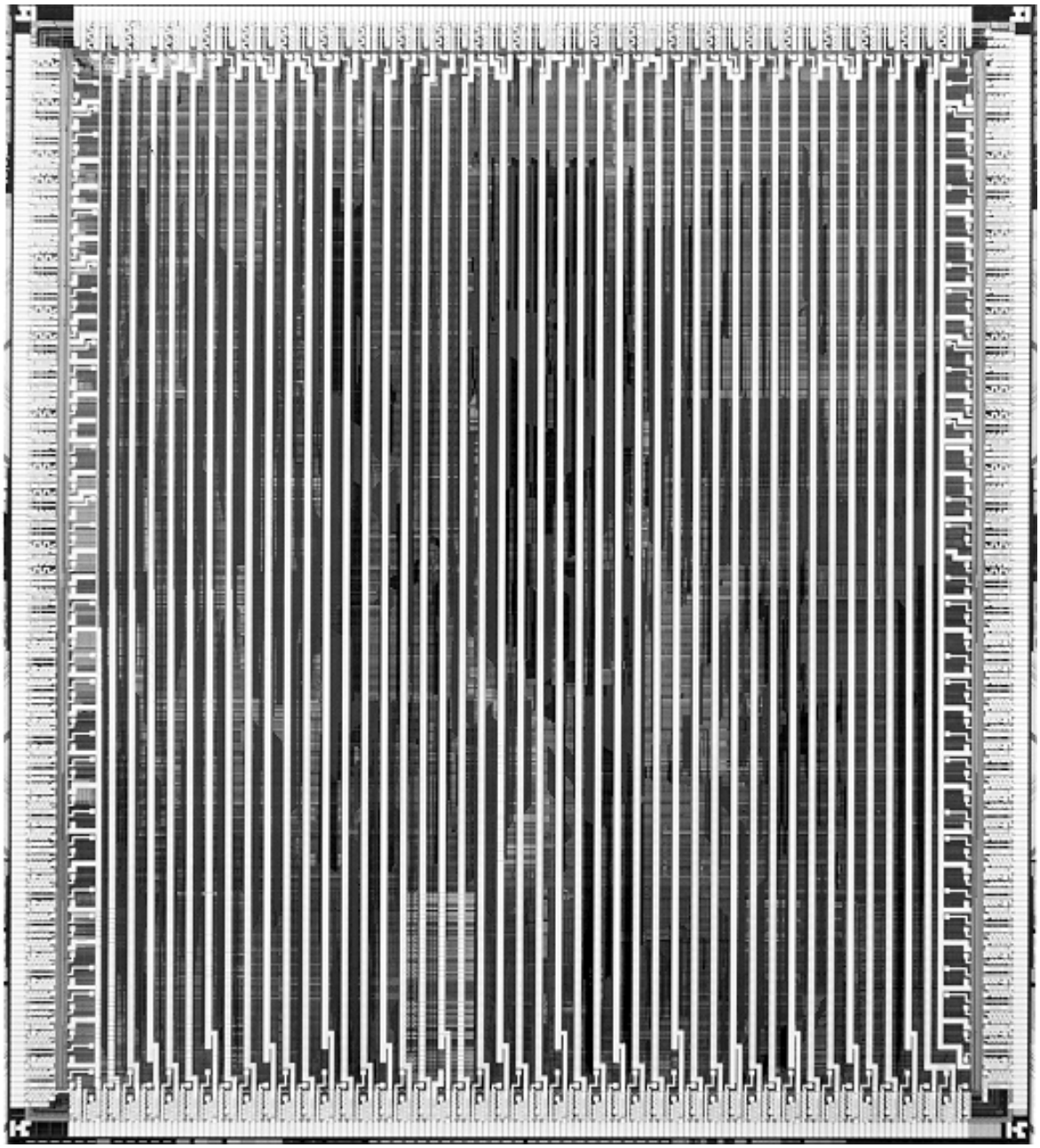


Figure 4: Cache RAM back side bus cache.



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